

## WHAT IS CLAIMED IS:

1 1. A frequency discriminator for detecting phase shifts  
2 between sequential pulses in a frequency-shift keyed (FSK) signal  
3 having a nominal frequency,  $f$ , said frequency discriminator  
4 comprising:

5 a first current controlled delay line capable of  
6 receiving said FSK signal and delaying said FSK signal by a  
7 desired time delay to thereby produce a time-delayed FSK signal;

8 a first multiplier capable of receiving and multiplying  
9 said FSK signal and said time-delayed FSK signal to thereby  
10 produce an output product signal proportional to a phase shift  
11 between said FSK signal and said time-delayed FSK signal; and

12 a delay locked loop comprising a second current  
13 controlled delay line substantially similar to said first current  
14 controlled delay line, wherein said delay locked loop receives a  
15 reference clock signal having a time period equal to said desired  
16 time delay and adjusts a control current level in said second  
17 current controlled delay line until a delay of said second  
18 current controlled delay line matches said time period of said  
19 reference clock signal, wherein said control current level is  
20 then used to adjust a delay of said first current controlled  
21 delay line.

1        2.    The frequency discriminator as set forth in Claim 1  
2 wherein said delay locked loop adjusts said control current level  
3 of said second current controlled delay line by adjusting a bias  
4 current in said second current controlled delay line.

1        3.    The frequency discriminator as set forth in Claim 2  
2 wherein said delay locked loop adjusts said delay of said first  
3 current controlled delay line by adjusting a bias current in said  
4 first current controlled delay line to match said bias current in  
5 said second current controlled delay line.

1        4.    The frequency discriminator as set forth in Claim 3  
2 wherein said delay locked loop comprises a phase detector having  
3 a first input for receiving said reference clock signal and a  
4 second input for receiving an output signal of said second  
5 current controlled delay line and generating a correction control  
6 signal determined by a phase difference between said reference  
7 clock signal and said output signal of said second current  
8 controlled delay line.

1        5.    The frequency discriminator as set forth in Claim 4  
2 wherein said second current controlled delay line is configured  
3 as an oscillator.

1        6.    The frequency discriminator as set forth in Claim 2  
2 further comprising:

3            a third current controlled delay line capable of  
4 receiving said FSK signal and delaying said FSK signal by a  
5 desired time delay to thereby produce a time-delayed FSK signal;  
6 and

7            a second multiplier capable of receiving and  
8 multiplying said FSK signal and said time-delayed FSK signal to  
9 thereby produce an output product signal proportional to a phase  
10 shift between said FSK signal and said time-delayed FSK signal;  
11 wherein said delay locked loop uses said control current level to  
12 adjust a delay of said third current controlled delay line.

1        7.    The frequency discriminator as set forth in Claim 6  
2 wherein said delay locked loop adjusts said delay of said third  
3 current controlled delay line by adjusting a bias current in said  
4 third current controlled delay line to match said bias current in  
5 said second current controlled delay line.

1 8. A frequency-shift keyed (FSK) receiver comprising:  
2 demodulation circuitry capable of receiving an incoming  
3 radio frequency (RF) signal and generating therefrom a frequency-  
4 shift keyed (FSK) signal having a nominal frequency,  $f_c$ ; and  
5 a frequency discriminator coupled to said demodulation  
6 circuitry for detecting phase shifts between sequential pulses in  
7 said FSK signal, said frequency discriminator comprising:  
8 a first current controlled delay line capable of  
9 receiving said FSK signal and delaying said FSK signal by a  
10 desired time delay to thereby produce a time-delayed FSK  
11 signal;  
12 a multiplier capable of receiving and multiplying  
13 said FSK signal and said time-delayed FSK signal to thereby  
14 produce an output product signal proportional to a phase  
15 shift between said FSK signal and said time-delayed FSK  
16 signal; and  
17 a delay locked loop comprising a second current  
18 controlled delay line substantially similar to said first  
19 current controlled delay line, wherein said delay locked  
20 loop receives a reference clock signal having a time period  
21 equal to said desired time delay and adjusts a control  
22 current level in said second current controlled delay line  
23 until a delay of said second current controlled delay line  
24 matches said time period of said reference clock signal,  
25 wherein said control current level is then used to adjust a

26 delay of said first current controlled delay line.

1 9. The frequency-shift keyed receiver as set forth in  
2 Claim 8 wherein said delay locked loop adjusts said control  
3 current level of said second current controlled delay line by  
4 adjusting a bias current in said second current controlled delay  
5 line.

1 10. The frequency-shift keyed receiver as set forth in  
2 Claim 9 wherein said delay locked loop adjusts said delay of said  
3 first current controlled delay line by adjusting a bias current  
4 in said first current controlled delay line to match said bias  
5 current in said second current controlled delay line.

1 11. The frequency-shift keyed receiver as set forth in  
2 Claim 10 wherein said delay locked loop comprises a phase  
3 detector having a first input for receiving said reference clock  
4 signal and a second input for receiving an output signal of said  
5 second current controlled delay line and generating a correction  
6 control signal determined by a phase difference between said  
7 reference clock signal and said output signal of said second  
8 current controlled delay line.

1 12. The frequency-shift keyed receiver as set forth in  
2 Claim 11 wherein said second current controlled delay line is  
3 configured as an oscillator.

1 13. The frequency-shift keyed receiver as set forth in  
2 Claim 9 further comprising:

3 a third current controlled delay line capable of  
4 receiving said FSK signal and delaying said FSK signal by a  
5 desired time delay to thereby produce a time-delayed FSK signal;  
6 and

7 a second multiplier capable of receiving and  
8 multiplying said FSK signal and said time-delayed FSK signal to  
9 thereby produce an output product signal proportional to a phase  
10 shift between said FSK signal and said time-delayed FSK signal;  
11 wherein said delay locked loop uses said control current level to  
12 adjust a delay of said third current controlled delay line.

1 14. The frequency-shift keyed receiver as set forth in  
2 Claim 13 wherein said delay locked loop adjusts said delay of  
3 said third current controlled delay line by adjusting a bias  
4 current in said third current controlled delay line to match said  
5 bias current in said second current controlled delay line.

1 15. A method of controlling a frequency discriminator  
2 operable to detect phase shifts between sequential pulses in a  
3 frequency-shift keyed (FSK) signal having a nominal frequency,  $f$ ,  
4 the method comprising the steps of:  
5 in a first current controlled delay line, delaying the  
6 FSK signal by a desired time delay to thereby produce a time-  
7 delayed FSK signal;  
8 in a multiplier, multiplying the FSK signal and the  
9 time-delayed FSK signal to thereby produce an output product  
10 signal proportional to a phase shift between said FSK signal and  
11 said time-delayed FSK signal;  
12 in a delay locked loop comprising a second current  
13 controlled delay line substantially similar to the first current  
14 controlled delay line, receiving a reference clock signal having  
15 a time period equal to the desired time delay and adjusting a  
16 control current level in the second current controlled delay line  
17 until a delay of the second current controlled delay line matches  
18 the time period of the reference clock signal; and  
19 adjusting a delay of the first current controlled delay  
20 line according to the control current level.

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1 16. The method as set forth in Claim 15 wherein the step of  
2 adjusting the control current level of the second current  
3 controlled delay line comprises the step of adjusting a bias  
4 current in the second current controlled delay line.

1 17. The method as set forth in Claim 16 wherein the step of  
2 adjusting the delay of the first current controlled delay line  
3 comprises the step of adjusting a bias current in the first  
4 current controlled delay line to match the bias current in the  
5 second current controlled delay line.

1 18. The method as set forth in Claim 17 wherein the delay  
2 locked loop comprises a phase detector having a first input for  
3 receiving the reference clock signal and a second input for  
4 receiving an output signal of the second current controlled delay  
5 line and generating a correction control signal determined by a  
6 phase difference between the reference clock signal and the  
7 output signal of the second current controlled delay line.

1 19. The method as set forth in Claim 18 wherein the second  
2 current controlled delay line is configured as an oscillator.



1 20. The method as set forth in Claim 16 further comprising  
2 the steps of:

3 in a third current controlled delay line, delaying the  
4 FSK signal by a desired time delay to thereby produce a time-  
5 delayed FSK signal;

6 in a second multiplier, multiplying the FSK signal and  
7 the time-delayed FSK signal to thereby produce an output product  
8 signal proportional to a phase shift between said FSK signal and  
9 said time-delayed FSK signal; and

10 adjusting a delay of the third current controlled delay  
11 line according to the control current level.

1 21. The method as set forth in Claim 20 wherein the step of  
2 adjusting the delay of the third current controlled delay line  
3 comprises the step of adjusting a bias current in the third  
4 current controlled delay line to match the bias current in the  
5 second current controlled delay line.